

ABSTRACT

A field effect transistor comprising: a semiconductor layer projecting from
15 the plane of a base; a gate electrode provided on opposite side surfaces of the
semiconductor layer; a gate insulating film interposed between the gate
electrode and the side surface of the semiconductor layer; and source/drain
regions where a first conductivity type impurity is introduced, wherein the
semiconductor layer has a channel forming region in a portion sandwiched
20 between the source/drain regions, and has in the upper part of the
semiconductor layer in the channel forming region a channel impurity
concentration adjusting region of which the concentration of a second
conductivity type impurity is higher than that in the lower part of the
semiconductor layer, and in the channel impurity concentration adjusting region,
25 a channel is formed in a side surface portion facing the gate insulating film of
the semiconductor layer in the channel impurity concentration adjusting region
in a state of operation in which a signal voltage is applied to the gate electrode.